Medium Size Backlight NCP5050: Drive Up to 120 LEDs (6 to 10 in Series Configuration)

ON Semiconductor®

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Prepared by: Hubert Grandry
Senior Applications Engineer

Introduction

CCFL lamps have been commonly used for backlighting medium sized 5” to 10” LCD panels in applications such as portable DVD players, electronic picture frames, and GPS navigation systems. As white LEDs efficiency continues to improve rapidly, they are now displacing CCFL for these panel sizes. White LED backlighting is attractive since it can result in thinner and lighter products. In addition since LEDs are more efficient they can improve battery life while offering a wider dimming range over CCFL lamps. This application note illustrates how the NCP5050 white LED driver can be configured to drive multiple LED strings for LCD backlighting and how to expand the output voltage rating beyond its 20 V rating to drive 6 LED to 10 LEDs in series.

In addition, this application note highlights how the NCP5050 can be easily configured to operate from 2 Cell Li-Ion batteries, NiMH battery packs, or from a 12 V automotive adapter.

Multi Branches Based on Current Mirror

The NCP5050 is a fixed frequency PWM boost converter optimized for driving a constant current through one string of high power LEDs. The basic application depicted on shows how to duplicate the constant current flowing through the primary branch to a secondary one. In addition, a capacitive doubler has been added to the output to expand the output voltage capability. The NCP5050 regulates a constant current I_1 in primary branch by maintaining 250 mV across the sense resistor R_{LCS}. This current I_1 is fixed by the Equation 1. For example, should one need 20 mA, R_{LCS} should be selected according to the following equation:

$$R_{LCS} = \frac{F_{BV}}{I_{OUTL}} = \frac{250\ mV}{20\ mA} = 12.5\ \Omega \qquad \text{(eq. 1)}$$

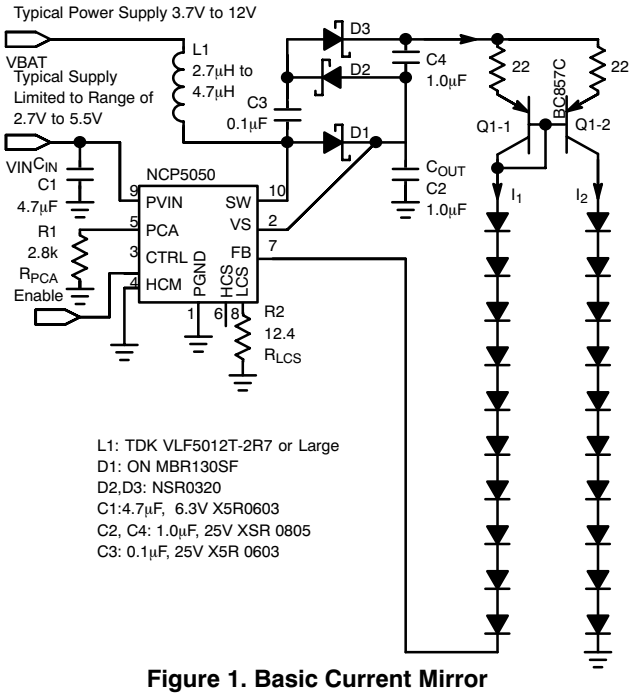

Figure 1. Basic Current Mirror

The secondary current I_2 is driven by the current mirror Q1-1 / Q1-2 and this current mirror has 1:1 ratio, so $I_1 = I_2$. The current mirror is realized with two small surface mount resistors and a single Dual PNP transistor in a very small SC88-6 lead package. For improved current matching a match pair PNP device in a very small SOT-563 package such as the NST30010MXV could be used.

As depicted on the current I_1 can be mirrored as many times as required. Total current I_T is the sum of current flowing through each (n) branch according to Equation 2:

$$I_T = n \times I \qquad \text{(eq. 2)}$$

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The maximum number of LEDs is determined by the NCP5050's output power capability which varies based on the given battery voltage (V_{BAT}), the total LEDs current (I_T) and selected external components. Note that the schematic in Figure 1 illustrates that the inductor can be powered directly from the battery or other power source while the NCP5050 V_{IN} input is maintained within it specified input range with a low power LDO or a current-limited zener regulator. This split power configuration is not required for 5 V and single cell Li-Ion power sources. Tables 1 to 3 illustrate the maximum number of LEDs branches based on the various LED string lengths that can be powered according to the available battery voltage and the components depicted on.

Table 1. TYPICAL OUTPUT CURRENT CAPABILITY
(I_T @ 10 LEDs in series (35 V))

Typ. V_{BAT} (V)	I_T (mA)	n Branches at 20 mA
12	240	12
7.4	176	8
5.0	128	6
3.7	72	3

Table 2. TYPICAL OUTPUT CURRENT CAPABILITY
(I_T @ 8 LEDs in series (28 V))

Typ. V_{BAT} (V)	I_T (mA)	n Branches at 20 mA
12	256	12
7.4	208	10
5.0	160	8
3.7	96	4

Table 3. TYPICAL OUTPUT CURRENT CAPABILITY
(I_T @ 6 LEDs in series (21 V))

Typ. V_{BAT} (V)	I_T (mA)	n Branches at 20 mA
12	288	14
7.4	240	12
5.0	160	8
3.7	112	5

Finally as demonstrated with statistical measurements in, we can see that typical current matching between strings is maintained within ±3% with the application schematic depicted on.

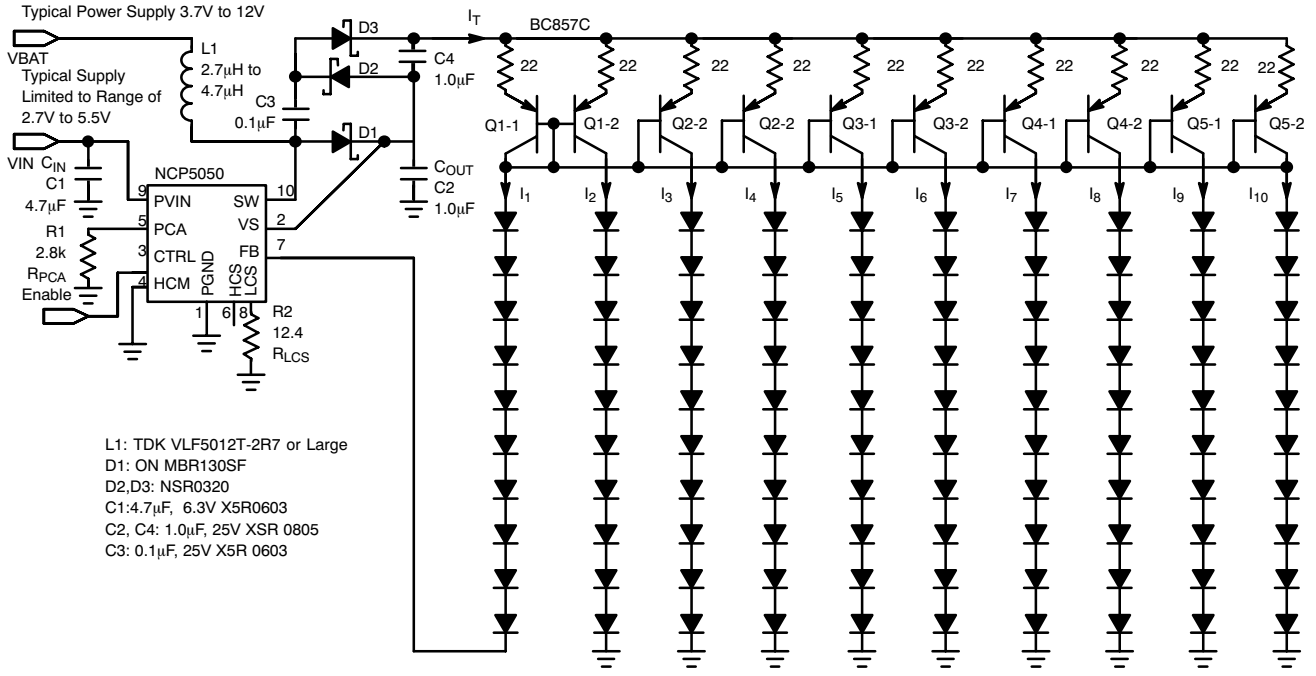

Figure 2. Multi Branches Current Mirror Schematic

Multi Branches with Ballast Resistor

If cost is of more concern than perfect matching, an inexpensive solution is depicted. This application schematic uses ballast resistors to match the LEDs current between strings. A good compromise is to use a ballast resistor of 68 Ω that gives 0.68 V drop at 10 mA and maintains losses within 2% to 3% for the 10 LED case illustrated. The total current (I_T) is controlled by R_{LCS} according to Equation 3 and distributed in all (n) branches according to Equation 4:

$$R_{LCS} = \frac{F_{BV}}{I_T} = \frac{250\ mV}{200\ mA} = 1.25\ \Omega \qquad \text{(eq. 3)}$$

$$I_1 = \frac{I_T}{n} \quad \text{(eq. 4)}$$

A circuit like usually achieves fairly good brightness matching if care has been taken in production to get forward voltage LEDs variation as low as possible. Usually the V_F LED-to-LED variation within a lot is fairly uniform and some LEDs manufacturers offer accurate binning tolerance of forward voltages. With this precaution, we obtain typical current matching within ±10% based on the statistical data shown in Figure 5.

Finally the total forward voltage in a given string is averaged by the quantity of LEDs in series which further improved the standard deviation of the current matching.

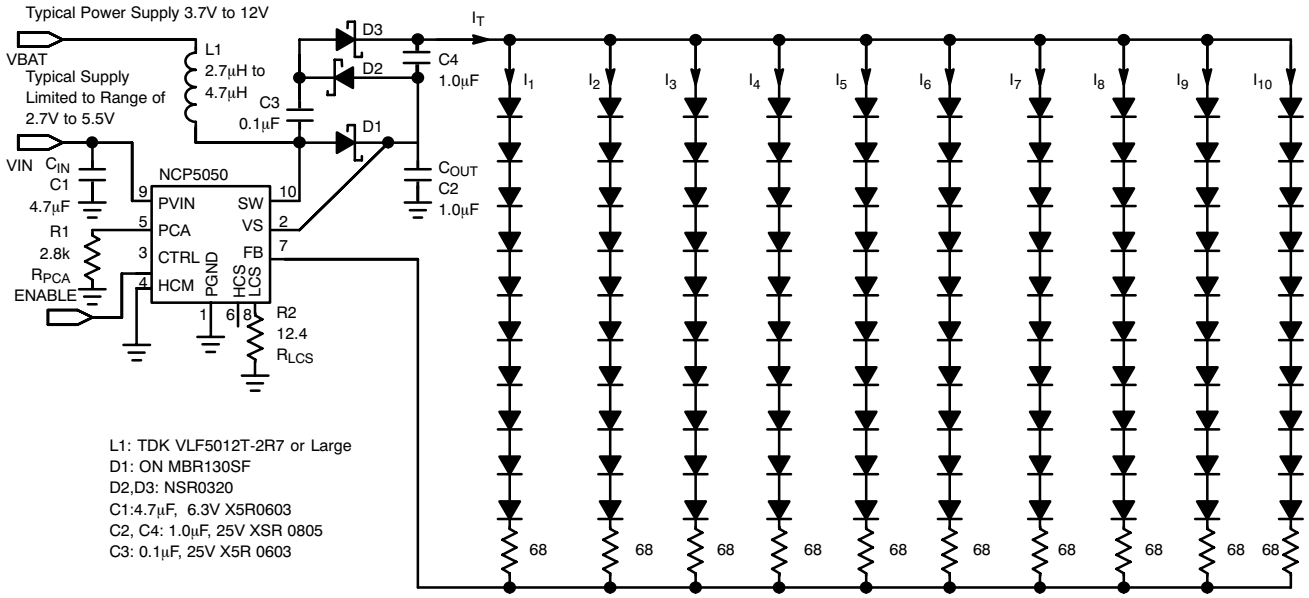

Figure 3. Multi Branches Ballast Resistor Schematic

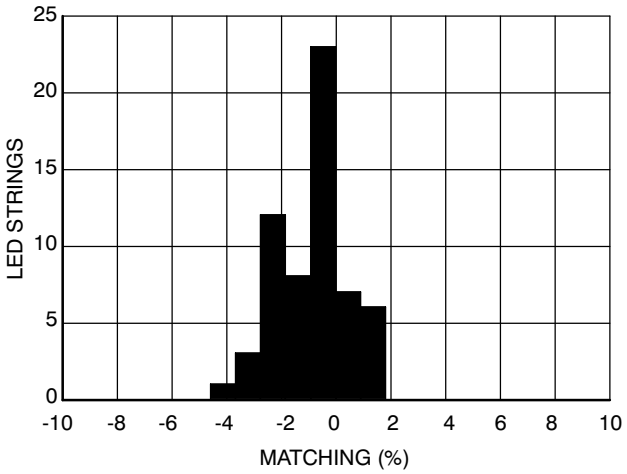

Figure 4. Current Matching over 60 Strings of LEDs with Current Mirror Schematic Depicted Figure 2

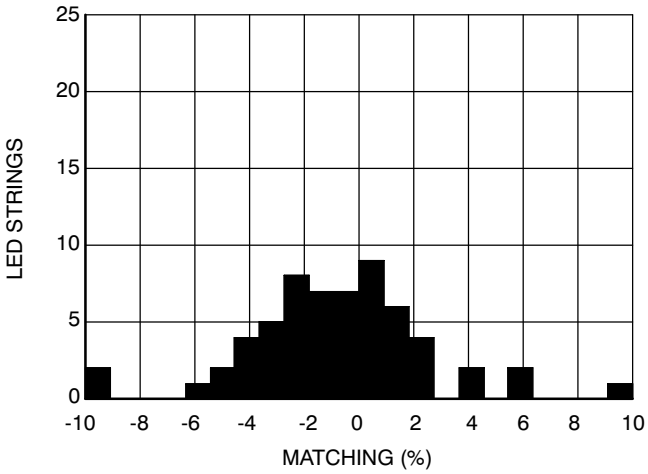

Figure 5. Current Matching over 60 Strings of LEDs without Current Mirror Depicted Figure 3

Voltage Doubler

The voltage doubler circuit is shown in. We can analyze it as two half-wave rectifier circuits in series. During the conduction of M1 V_{SW} is pulled down to zero volts, the diodes D1 and D3 are open and the diode D2 conducts and charges the capacitor C3. During the second phase D1 and D3 are conducting to charge C2 and C4. The V_{OUT} voltage across the combination is therefore equal to twice the V_{SW} peak voltage minus the forward voltage of D1, D2 and D3. A few voltage doubler operation cycles are depicted.

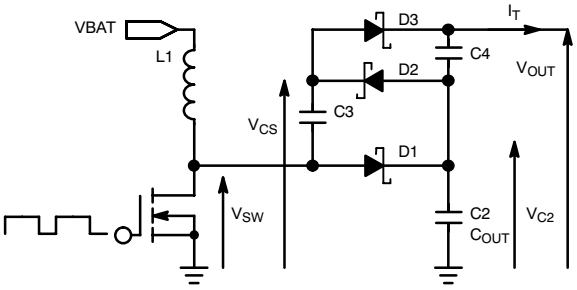

Figure 6. Voltage Doubler Schematic

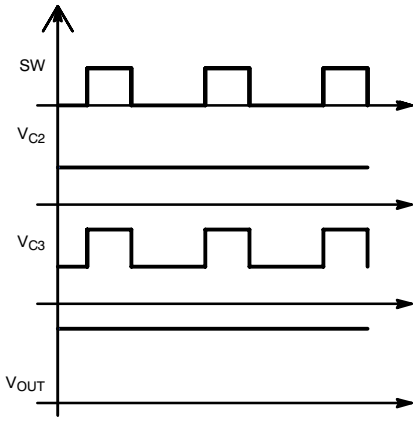

Figure 7. Voltage Doubler Operation

Due to the NCP5050's high switching frequency, this type of circuit can supply a significant current (I_T) to the load with small discrete components and very good efficiency. Some recommended components include but are not limited to the following:

D1:
ON Semiconductor: MBR130LSFT1G,
ON Semiconductor: MBR120LSFT3G

D2, D3:
ON Semiconductor: NSR0320MW2T

C2, C4:
1.0 μF 25 V 0805
TDK: C2012X5R1E105M

C3:
0.1 _F 50 V 0603
TDK: C1608X5R1H104M

Dimming Technique

The best and simplest way to dim the LED brightness is to use a pulse width modulation technique. The PWM signal is applied to CTRL input and thereby the mean load current of the LEDs is proportional to the duty cycle (see). In other words by reducing the duty cycle the brightness of the LEDs is dimmed. This application with a voltage doubler supports PWM dimming frequencies up to 50 kHz. To avoid any optical flicker switching or audible noise the frequency must should be in the range of 100 Hz - 500 Hz or 20 kHz - 50 kHz.

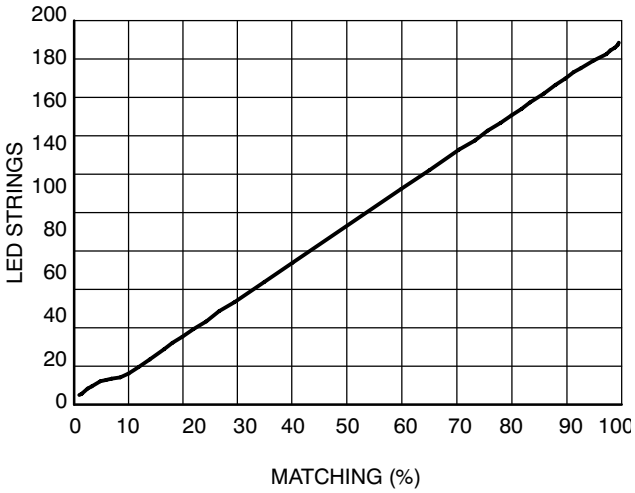

Figure 8. I_T Mean vs. Duty Cycle

TYPICAL OPERATING CHARACTERISTICS

Efficiency = 100 x (V_{LEDS} x I_T)/Pin

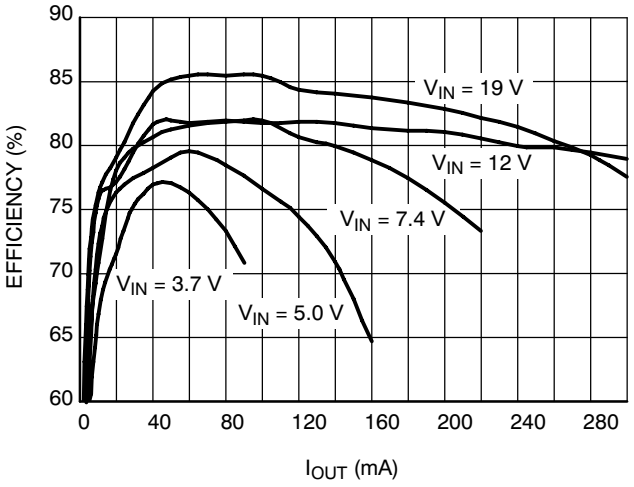

Figure 9. Efficiency vs. Total Output Current I_T @ 10 LEDs (35 V) L1 = TDK VLF5012A-2R7

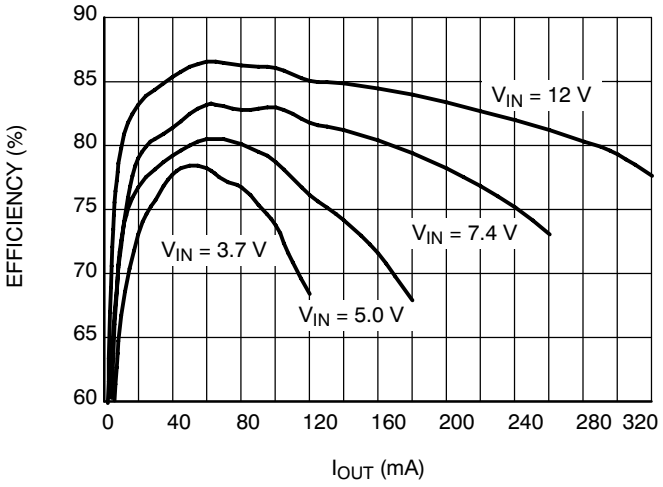

Figure 10. Efficiency vs. Total Output Current I_T @ 8 LEDs (28 V) L1 = TDK VLF5012A-2R7

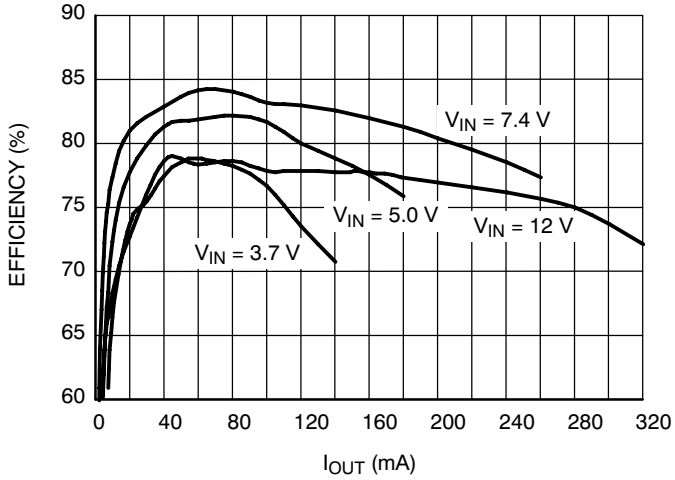

Figure 11. Efficiency vs. Total Output Current I_T @ 6 LEDs (21 V) L1 = TDK VLF5012A-2R7

Evaluation Board

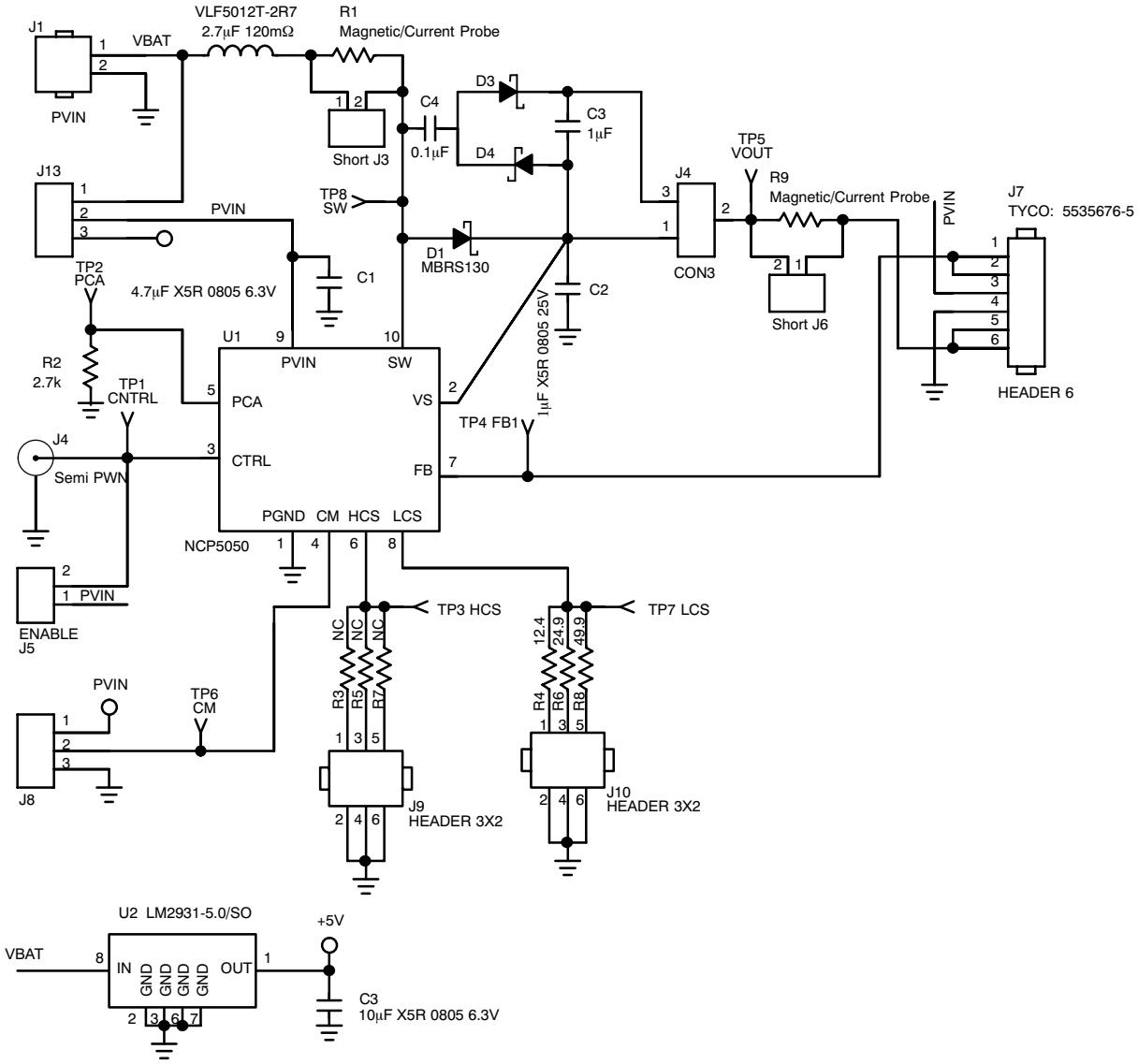

Figure 12. NCP5050EVB3/D Schematic

Operation

NCP5050 operating power supply ranges from 2.7 V to 5.5 V. The absolute maximum input voltage is 7.0 V. However an LM2931-5.0 has been embedded to deliver + 5.0 V to the NCP5050 when battery voltage is above 5.5 V (see J13 position). Thereby this application can typically operate up to 12 V and withstands up to 19 V but we have to keep in mind that the output voltage should always be above or equal to the input voltage to remain in boost operation. The power supply current limit should set to >3 A and is connected to J1 connector to power the NCP5050EVB3/D. Also to compensate for the wires' parasitic inductance between the power supply and the evaluation board it is highly recommended to connect 470 μF electrolytic capacitor to bypass J1 terminal. By doing so, the device can be evaluated under conditions very similar to when powered from a battery.

Evaluation Board Performance

To maintain a small footprint, the design of this solution uses small size components whenever possible. Changing components may positively or negatively impact the performance illustrated in Figures 6 through 8. For example, should one change inductors: a larger one having a lower DCR or/and higher value (in micro Henri) may improve efficiency. Changing the Schottky diode D1, D3 or D4 could move the quiescent current and impact the efficiency. For more information please refer to the NCP5050 datasheet.

INPUT POWER

Symbol	Descriptions
J1-1	This is the positive connection for power supply. The leads (positive + ground) to the input supply should be twisted and kept as short as possible.
J1-2	This is the return connection for the power supply (Ground signal)
J2, J11	Ground clip

OUTPUT POWER

Symbol	Descriptions
J7-1/2	This is the positive output connection (V_{OUT}) of the boost converter.
J7-5/6	This is the return connection for load current to FB Pin.
J7-3	This is the return connection for load current to the ground.
J7-4	This is an optional connection for P_{VIN} to the daughter board.

SWITCHES SETUP

Symbol	Switch Descriptions
J4	PWM DIM: This connector should be used to demonstrate PWM dimming of the LED string. In that case, jumper J5 must be left OPEN for proper operation. When a digital signal with a high logic level is applied to this terminal the device is enabled. By varying the duty cycle of this signal, the average LED current can be reduced thus dimming the LEDs brightness. The frequency of this signal can be up to 50 kHz.
J5	ENABLE: To enable the boost converter connect a shorting jumper between J5-1 and J5-2
J8-1/2/3	CM: Open (Not used in this application)
J13-1/2	Placing a shorting jumper bypasses the 5.0 V regulator and connects NCP5050's P_{VIN} directly to V_{BAT}.
J13-2/3	Placing a shorting jumper connects NCP5050's P_{VIN} to the + 5.0 V of the embedded LDO.
J14-1/2	Placing a short connect directly the output of the NCP5050 and bypasses the voltage double circuit of D3, D4, C4 and C5.
J14-2/3	Placing a short connects the output of the voltage doubler to the output connector J7.

OUTPUT CURRENT SETUP

Switch J10 setup the output current from 0 to 35 mA for torchlight mode (LCS pin) following table below.

J10-1/2	J10-3/4	J10-5/6	I_{OUT} (mA) Flashlight Mode (LCS)
0	0	0	0
0	0	1	5.0
0	1	0	10.0
0	1	1	15.0
1	0	0	20.0
1	0	1	25.0
1	1	0	30.0
1	1	1	35.0

0 = Open
1 = Shorting jumper connected

TEST POINT

Symbol	Switch Descriptions
TP1	This test point is connected to the CTRL input pin.
TP2	This test point is connected to the PCA pin signal.
TP3	This test point is connected to the HCS pin signal (No used in this application)
TP4	This test point is connected to the FB pin signal.
TP5	This test point is connected to the output voltage of this application.
TP6	This test point is connected to the CM input pin (No used in this application)
TP7	This test point is connected to the LCS pin signal.
TP8	This test point is connected to the SW pin signal.
R1	This test point is used to monitor with an oscilloscope the current through the L1 inductor thanks to a DC current probe when J3 is open.
R9	This test point is used to monitor the load current when J6 is open.

PCB Layout

As with all switching DC/DC converters, care must be observed to place the components on the PCB and to layout the critical nodes. The noise-sensitive feedback (FB) path has been isolated from the SW node which is carrying high-frequency switching current. Also in order to provide EMI behavior similar to a mass production application, the evaluation board is made of 4 PCB layers where the first internal layer is a GND plane 90 μm from to top. , and show the layout of the NCP5050EVB board.

For more specific layout guidelines please refer to the NCP5050 datasheet.

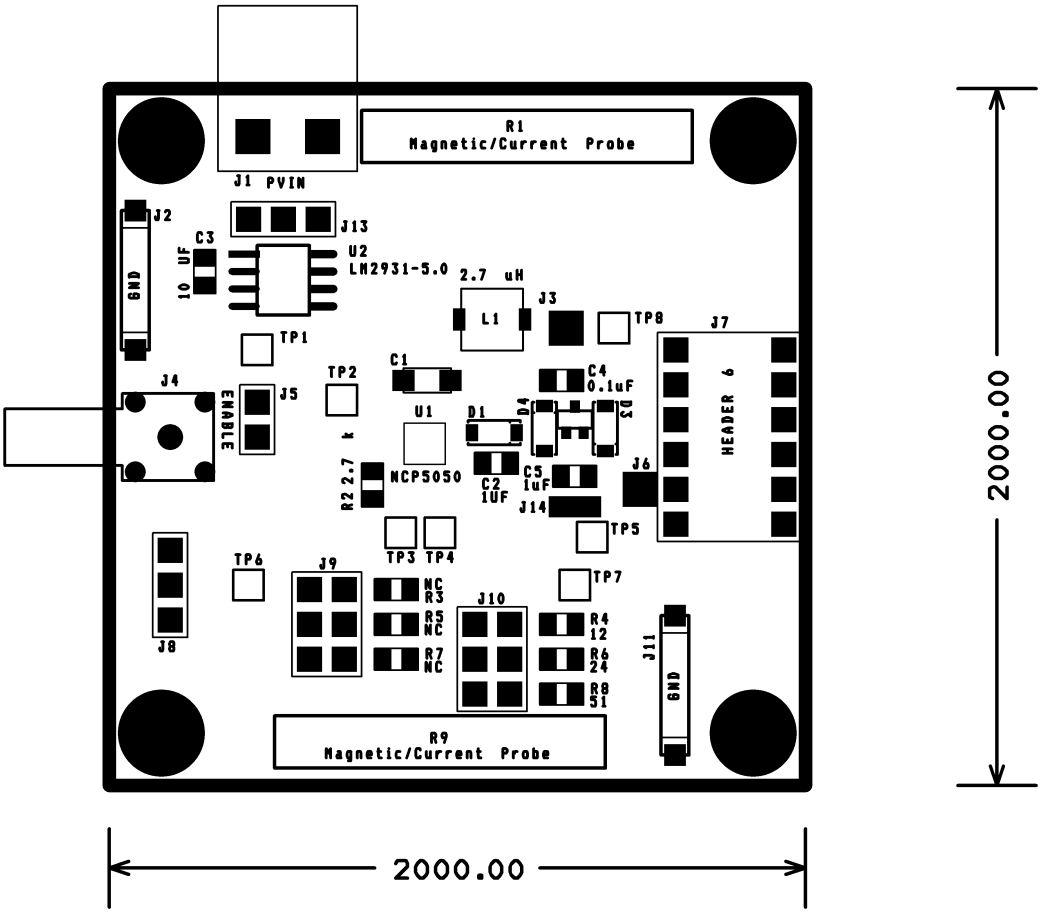

Figure 13. Assembly Layer

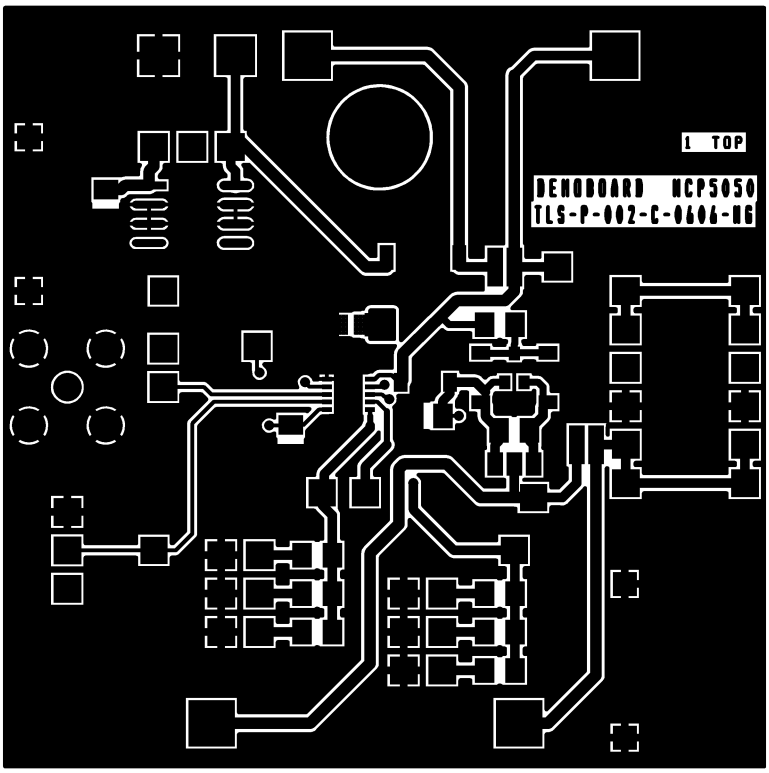

Figure 14. Top Layer Routing

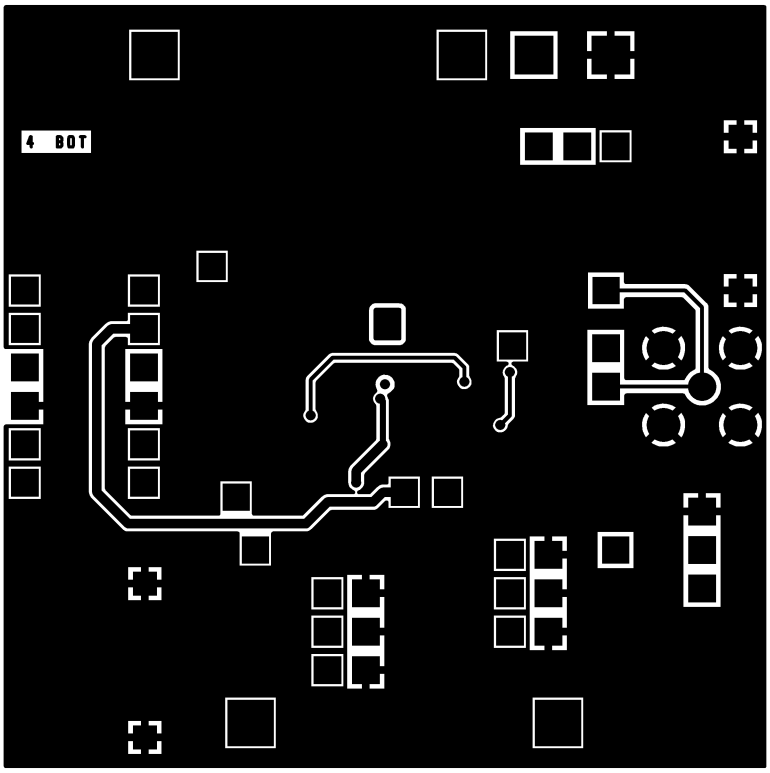

Figure 15. Bottom Layer Routing

BILL OF MATERIALS

Qty	Ref Des.	Description	Size	Manufacturer	Part Number
1	U1	4.5 W Flash LED Boost Driver	10-Pin DFN 3 x 3 x 1.0	ON Semiconductor	NCP5050
1	U2	5 V LDO Voltage Regulator	SOIC-8	ON Semiconductor	LM2931AD-5.0
1	C1	Capacitor, Ceramic 4.7 μF 6.3 V	0603	TDK	C1608X5R0J475M
1	C2,C5	Capacitor, Ceramic 1.0 μF 25 V	0805	TDK	C2012X5R1E105M
1	C3	Capacitor, Ceramic 10 μF 6.3 V	0805	TDK	C2012X5R0J106M
1	C4	Capacitor, Ceramic 0.1 μF 50 V	0805	TDK	C1608X5R1H104M
1	D1	Schottky Diode 1A 30 V	SOD-123FL	ON Semiconductor	MBR130LSFT1G
1	D3,D4	Schottky Diode	SOD-323	ON Semiconductor	NSR0320MW2T1G
1	L1	Inductor, SMT, 2.7 μH, 2.0 A, 100 mΩ or Inductor, SMT, 3.3 μH, 4.1A, 20 mΩ	4.5 x 4.7 x 1.2 mm 7.3 x 7.3 X 3.2 mm	TDK	VLF5012 -2R7 RLF7030T-3R3M4R1
1	R1, R9	Loop of 4 cm wire	-	Std	Std
1	R2	Resistor, Chip, 2.7 kΩ, 1%	0603	Std	Std
	R3,R5,R7	Not Connected	0603	Std	Std
2	R4	Resistor, Chip, 12.4 Ω, 1%	0603	Std	Std
2	R6	Resistor, Chip, 24.9 Ω, 1%	0603	Std	Std
2	R8	Resistor, Chip, 49.9 Ω, 1%	0603	Std	Std
1	J1	Mal. SL5.08/2/90B plus Fem. BLZ 5.08/2	-	Weidmuller	SL5.08/2/90 + BLZ 5.08/2
2	J2,J11	GND Connection	-	Std	Std
3	J3,J6 J14	Optional Short	-	-	-
1	J4	Optional SMA / SMB Connector	-	-	-
1	J5	Header 2 pin, 100 mil spacing	0.100 x 2	Std	Std
1	J7	AMPMODU Mod II Right-Angle Horizontal PCB Connector		Tyco	5535676-5
1	J13	Header 3 pin, 100 mil spacing	0.100 x 3	Std	Std
2	J8,J9	Not Connected	-	-	-
1	J10	Header 2X3 pin, 100 mil spacing	0.100 x 2 x 3	Std	Std
6	TP1,2,4,5,7,8	Test Point	-	Std	Std
2	TP3,6	Optional Test Point	-	Std	Std
1	PCB	PCB 2.0 in x 2.0 in x 1.0 mm, 4 Layers	-	Any	TLS-P-002-C-0606-HG

CURRENT MIRROR DAUGHTER BOARD

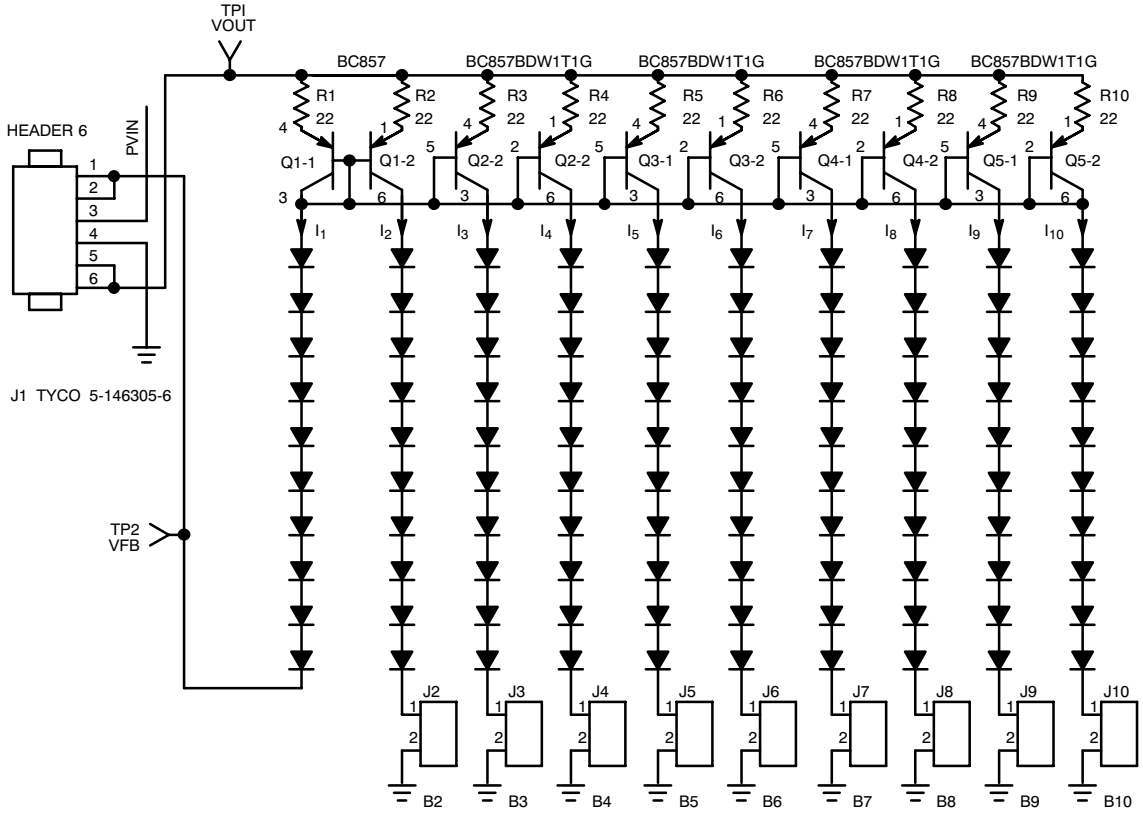

Figure 16. 10X10LED_CMDB/D Schematic

INPUT POWER

Symbol	Descriptions
J1-1/2	This is the return current of the primary string.
J1-3	This is the return connection for the power supply (Ground signal)
J1-4	P_{VIN} signal from the NCP5050EVB3 Board.
J1-5/6	This is the positive output connect from the NCP5050EVB3 board.

This connector must connect to J7 of NCP5050EVB3.

SWITCHES SETUP

Symbol	Switch Descriptions
J2 to J10	This switch is used to insert and ampere meter in corresponding string to measure the current flowing.

TEST POINT

Symbol	Switch Descriptions
TP1	This test point is connected to the output voltage from the NCP5050EVB3 board.
TP2	This test point is connected to the FB pin signal.

BILL OF MATERIALS

Qty	Ref Des.	Description	Size	Manufacturer	Part Number
10	R1 to R10	Resistor, Chip, 22 Ω, 5%	0805	Std	Std
5	Q1 to Q5	Dual PNP Transistors	SC88-6	ON Semiconductor	BC857CDW1T1G
100	D101 to D200	Side White LED		OSRAM	LW Y87S or LW Y1SG
9	J2 to J10	Header 2 pin, 100 mil spacing	0.100 x 2	Std	Std
2	TP1,2	Test Point	-	Std	Std
1	J1	.100x6 inch AMPMODU Headers Square Right-Angle Connector	-	Tyco	5-146305-6

BALLAST RESISTOR DAUGHTER BOARD

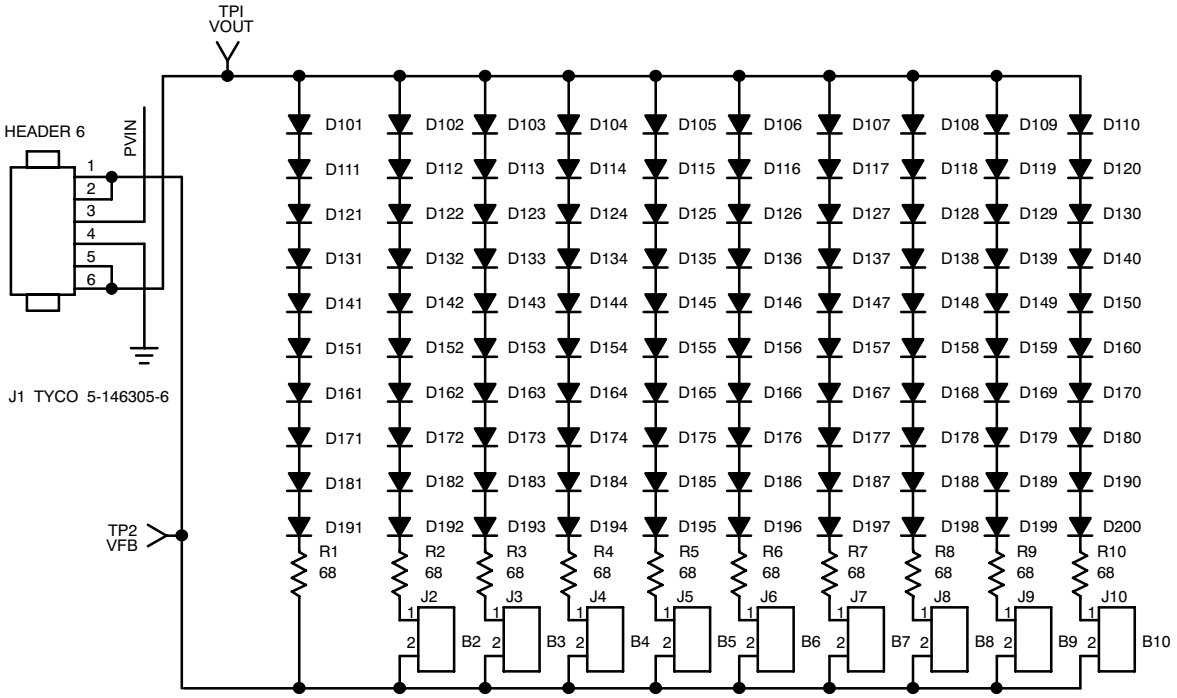

Figure 17. 10X10LED_BRDB/D Schematic

INPUT POWER

Symbol	Descriptions
J1-1/2	This is the return current of the total current.
J1-3	This is the Ground signal.
J1-4	P_{VIN} signal from the NCP5050EVB3 Board.
J1-5/6	This is the positive output connect from the NCP5050EVB3 board.

This connector must connect to J7 of NCP5050EVB3.

SWITCHES SETUP

Symbol	Switch Descriptions
J2 to J10	This switch is used to insert and ampere meter in corresponding string to measure the current flowing.

TEST POINT

Symbol	Switch Descriptions
TP1	This test point is connected to the output voltage from the NCP5050EVB3 board.
TP2	This test point is connected to the FB pin signal.

BILL OF MATERIALS

Qty	Ref Des.	Description	Size	Manufacturer	Part Number
10	R1 to R10	Resistor, Chip, 22 Ω, 5%	0805	Std	Std
100	D101 to D200	Side White LED		OSRAM	LW Y87S or LW Y1SG
9	J2 to J10	Header 2 pin, 100 mil spacing	0.100 x 2	Std	Std
2	TP1,2	Test Point	-	Std	Std
1	J1	.100x6 inch AMPMODU Headers Square Right-Angle Connector	-	Tyco	5-146305-6

PUBLICATION ORDERING INFORMATION

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